

## CS610 Computer Architecture

## Prof.Ennoure

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**Course Description**

This course provides students with a solid understanding of fundamental architectural techniques used to build today's high-performance processors and systems. The course also highlights the evolution of computer architecture and the factors influencing the design of hardware and software elements of a computer systems. Variety of topics in computer architectures will be covered including computer logic, x86, ARM architecture, RISC, bus designs, ISA, performance, cache and internal memeory, processor control, I/O, parallel processing and multithreading. It also addresses microarchitecture issues such as dynamic instruction scheduling, branch instruction, cache allocation, instruction-level parallelism, fetching, and multicore computing. Verification issues with today’s microprocessors are also outlined.

**Prerequisites**

None

**Learning Objectives**

The students will:

1. Identify and calculate quantitative measurements of the values of important characteristics of computer designs such as performance and dependability.
2. Define instruction level parallelism, relate it to pipelining and describe how a pipeline increases the throughput of a computer processor and calculate the throughput without stalls and with stalls.
3. List and describe techniques for branch prediction including static and dynamic methods and describe how they are integrated in a typical system.
4. Compare instruction level parallelism with thread-level parallelism and describe fine-grained multithreading, course-grained, and simultaneous multithreading.
5. Describe shared-memory multiple processor architectures, the cache coherence problem associated with them, and various protocols used to deal with the cache coherence problem.
6. Design a memory hierarchy by analyzing the performances of various alternatives to satisfy the required cost-performance specifications.
7. Compare the architecture design of x86 family processors with the ARM processors

**Course Materials**

Text: Computer Organization and Architecture, By William Stallings; ISBN: 13: 978-0-134-10161-3. Tenth Edition 2016; publisher : Pearson.

### Attendance Policy

Students are expected to attend every class of every course in which they are registered. Each class meeting provides a unique opportunity for learning. While acknowledging the critical importance of class attendance, the College also recognizes that there are times when absence from class is unavoidable. More than two absences in a course will result in the reduction of the student’s final grade by a full letter (for example from A to B).

### Accommodative Services

[Monroe College](https://webmail.monroecollege.edu/owa/redir.aspx?C=lydIE-uQIkm_ZOW-wbgr1rI6FvMz4NMIpmhnrK1qPPMdEJP5VWal5jPoRRriWfDs5XFUYcjNuQg.&URL=http%3a%2f%2fmonroecollege.smartcatalogiq.com%2fcurrent%2fUndergraduate-Catalog%2fStudent-Services%2fStudents-With-Disabilities) is accessible to students with disabilities and admits those students whose credentials demonstrate they have the motivation and capabilities to successfully pursue their academic goals at the college. All students with disabilities have access to a Coordinator of Services [for Students](https://webmail.monroecollege.edu/owa/redir.aspx?C=lydIE-uQIkm_ZOW-wbgr1rI6FvMz4NMIpmhnrK1qPPMdEJP5VWal5jPoRRriWfDs5XFUYcjNuQg.&URL=http%3a%2f%2fmonroecollege.smartcatalogiq.com%2fcurrent%2fUndergraduate-Catalog%2fStudent-Services%2fStudents-With-Disabilities) with Disabilities on each campus:

*Bronx Campus:                    Elizabeth Maybruch* [*emaybruch@monroecollege.edu*](https://webmail.monroecollege.edu/owa/redir.aspx?C=lydIE-uQIkm_ZOW-wbgr1rI6FvMz4NMIpmhnrK1qPPMdEJP5VWal5jPoRRriWfDs5XFUYcjNuQg.&URL=mailto%3aemaybruch%40monroecollege.edu)

*New Rochelle Campus:     Saadia Del-Lano;* [*sdellano@monroecollege.edu*](https://webmail.monroecollege.edu/owa/redir.aspx?C=lydIE-uQIkm_ZOW-wbgr1rI6FvMz4NMIpmhnrK1qPPMdEJP5VWal5jPoRRriWfDs5XFUYcjNuQg.&URL=mailto%3asdellano%40monroecollege.edu)

## **Final Grade:**

|  |  |
| --- | --- |
| **ACTIVITIES** | **% of Grading** |
| Homework/Reflections | 15 % |
| Research Paper/Project | 20 % |
| Exams | 40 % |
| Final Exam | 25 % |
| **TOTAL** | **100 %** |

**Topics Outline**

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| --- | --- | --- |
| **Date** | **Class Topic/Description** | **Activities and/or Assignments** |
| Week 1 | Basic Concepts and Computer Evolution   * Organization and Architecture * Structure and function * Brief History of computers * Evolution of Intel x86 Architecture * Embedded Systems * Arm Architecture * Could computing | Chapter 1 |
| Week 2 | Performance Issues   * Designing for performance * Multicore, Mics and GPGUs * Basic measures of Computer Architecture * Calculating the mean * Benchmarks and Spec | Chapter 2 |
| Week 3 | A top level view of computer function and interconnection   * Computer components * Computer functions * Interconnection structures * Point-to-point interconnect * PCI express | Chapter 3 |
| Week 4 | **EXAM 1** |  |
| Week 5 | Cache Memory   * Computer memory system overview * Cache memory principles * Elements of Cache design * Pentium 4 Cache organization | Chapter 4 |
| Week 6 | Internal Memory   * Semiconductor Main Memory * Error correction * DDR DRAM * Flash Memory * Newer Nonvolatile Solid-State memory technologies | Chapter 5 |
| Week 7 | Input/Output   * External Devices * I/O modules * Programmed I/O * Interrupt-Driven * Direct Memory/Cache Access * I/O channels and processors | Chapter 7 |
| Week 8 | Instruction Sets : Characteristics and functions   * Machine Instruction characteristics * Types of Operands * Intel x86 and ARM data types * Types of operations * Intel x86 and ARM operations | Chapter 12 |
| Week 9 | Instruction Sets: Addressing Modes and Formats   * Addressing Modes * X86 and ARM Addressing modes * Instruction format * X86 and ARM instruction format * Assembly language | Chapter 13 |
| Week 10 | **MID-TERM EXAM** |  |
| Week 11 | Processor Structure and function   * Processor organization * Register organization * Instruction cycle * Instruction pipelining * The x86 Processor family * The ARM Processor | Chapter 14 |
| Week 12 | Reduced instruction set computers   * Instruction execution characteristics * Reduced instruction set architecture * RISC pipelining * MIPS R4000 * RISC versus CISC controversy | Chapter 15 |
| Week 13 | Intruction\_level parallelism and superscalar Processors   * Overview * Design issues * Intel core microarchitecture * ARM Cortex-A8 | Chapter 16 |
| Week 14 | Parallel Processing   * Multiple processor organizations * Symmetric multiprocessors * Multithreading and chip multiprocessors * Cache Coherence * Nonuniform Memory Access. * Clusters * Cloud computing | Chapter 17 |
| Week 15 | **FINAL EXAM** |  |